REMARKS

Claims 1-34 are pending in the application. The Examiner objects to claim 16 for an informality. The Examiner rejects claims 1-10, 16, 21-34 under 35 U.S.C. §102(b) as being anticipated by Self et al. (US Patent No. 5,623,644). The Examiner rejects claims 11-15 under 35 U.S.C. §103(a) as being unpatentable over Self as applied to claim 10 in view of Tanaka et al. (US Patent No. 5,794,020). Applicant amends claims 1, 3, 5, 10, 16, 21, and 28. Claims 1-34 remain in the case. Applicant adds no new matter and requests reconsideration.

Claim Objections

Applicant amends claim 16 to obviate the Examiner's objection.

Claim Rejections Under § 102(b)

The Examiner rejects claims 1-10, 16, 21-34 as being anticipated by Self. Applicant respectfully traverses the Examiner's rejection.

Claim 1 recites *an adjustable delay element coupled to receive a clock signal and delaying said clock signal according to a phase difference between said clock signal and said data stream to derive said reference signal.* Claim 16 recites a similar limitation.

The Examiner alleges Self's digital delay lock loop circuit DDLL 320 discloses the recited adjustable delay element. DDLL 320, however, "provides the correct set up and hold time for the data by positioning the clock edge...midway in the dam [sic] cell.... The delay element control voltage over line 403 to the delay elements 401 and 402 step slowly until the delay through the two delay blocks matches one-half the period of the actual communication clock received over 302." Self, column 7, lines 40-48. That is, Self delays the communication clock 101 not according to the *phase difference between said clock signal and said data stream.* Self, Figure 4 and column 7, lines 44-53. And Self receives communication clock 101 and data 102 "in phase," and thus does not derive the recited reference signal according to *phase difference* between the communication clock 101 and data 102 as recited. Self, column 6, lines 49-63; Figure 4; and column 7, lines 44-53. Self, therefore, does not anticipate claim 1, or claim 16, and their corresponding dependent claims.

Claim 16 recites *a signal generating including a delay locked loop coupled to receive a reference signal, said delay locked loop generating said plurality of latching control signals responsive to said reference signal.* Claims 9, 27 and 28 recite similar limitations.

The Examiner alleges Self's DDLL 320 discloses the recited delay locked loop. But in his analysis of claim 1, the Examiner alleged the DDLL 320 disclosed the recited adjustable delay element 320 and the write pointer 330 disclosed the recited signal generator. Claim 16 recites that the signal generator includes a delay locked loop. The claim language as interpreted by the Examiner, therefore, would require the write pointer 330 to include the delay locked loop recited. It does not. Further, the claim language requires the signal generator and its included delay locked loop to *receive a reference signal* and to generate *said plurality of latching control signals*. In Self, the DDLL320 does not receive the signal 304, rather it provides it to the write pointer 330. And the DDLL 320 does not generate or otherwise provide the plurality of latching control signals as recited. In short, Self does not disclose the invention recited in claim 16 or claims 9, 27 and 28, and their corresponding dependent claims.

Claim 1 recites *where the latching control signals are offset.* Similarly, claim 16 recites *where the latching control signals are offset by substantially one data period.* Claim 21 recites a similar limitation.

The Examiner appears to allege that the output of Self's write pointer 330 discloses the recited a plurality of latching control signals. But the write pointer is a delayed version of communication clock 101, not a *plurality* of latching control signals *offset by substantially one data period.* Self, Figures 4 and 7; column 7, lines 44-53; and column 8, 51-64. Although Self's Figure 3 shows multiple connections between data latches 360 and write pointer 330, Self says nothing to describe these multiple connections and shows only a single write pointer at Figure 7. Self, Figure 7 and column 8, lines 51-64. Since Self does not enable a plurality of latching control signals, much less teach or suggest *latching control signals offset by substantially one data period*, Self does not disclose or enable the recited signal generator. Self, therefore, does not anticipate claims 1, 16, or 21 or their corresponding dependent claims.

Claim 28 recites *a delay locked loop coupled to receive a reference signal ... where the reference signal is a variably delayed signal.* The Examiner alleges Self's digital delay lock loop circuit DDLL 320 discloses the recited delay locked loop. DDLL 320, however, does not receive a delayed signal, much less a signal that is variably delayed. Self, therefore, does not anticipate claim 28 and its corresponding dependent claims.

Claim Rejections Under § 103(a)

The Examiner rejects claims 11-15 as being unpatentable over Self in view of Tanaka. Applicant respectfully traverses the Examiner's rejection.

Claim 11 recites *a fixed delay element coupled to receive at least one of said latching control signals and providing a delayed latching signal.* The Examiner appears to allege Tanaka's fixed delay circuit 3 or 4 and internal clock line 132 discloses the recited fixed delay element and latching control signals. Fixed delay circuits 3 and 4, however, do not receive internal clock line 132. Since fixed delay circuit 3 or 4 receives data, not latching control signals, Tanaka, therefore, does not anticipate claim 11 or its corresponding dependent claims.

Even if Tanaka taught the recited fixed delay element and latching component, this combination would not have provided motivation for "increased reliability of data transfers at high frequencies" as suggested by the Examiner since Self's digital delay lock loop circuit DDLL 320 does not receive any data to be latched, nor have any use for latched data. In other words, since DDLL 320 delays a communication clock according to its period, Self provides no motivation for DDLL 320 to receive data and latch the received data. Thus combining the references, as the Examiner suggests, is to no avail. Applicant therefore respectfully requests that this rejection be withdrawn and the pending claims be allowed to issue.

Claims 17-20

The Examiner does not allege, nor can Applicant ascertain at the time of this writing, where the references disclose the subject matter of claims 17-20. Applicant respectfully requests the Examiner to provide guidance.

CONCLUSION

For the foregoing reasons, the Applicant requests reconsideration and allowance of all claims as amended. The Applicant encourages the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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